What is claimed is:

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1. A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a first region of a first conductivity type;

a second region of a second conductivity type formed selectively in the surface portion of the first region;

a third region of the first conductivity type formed selectively in the surface portion of the first region, the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

a fifth region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the fifth region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the fifth region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other.

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2. The semiconductor device according to Claim 1, wherein the depths of the sub-regions of the fifth region are different from each other.

3. The semiconductor device according to Claim 1, wherein the gate electrode is extended onto the first insulation film.

4. A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first region of a first conductivity type formed selectively in the surface portion of the semiconductor substrate;

a second region of the second conductivity type formed selectively in the surface portion of the semiconductor substrate;

a third region of the first conductivity type formed selectively in the surface portion of the first region;

the second region and the third region being spaced apart from each other;

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a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

a fifth region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the fifth region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the fifth region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other.

5. The semiconductor device according to Claim 4, wherein the depths of the sub-regions of the fifth region are different from each other.

6. The semiconductor device according to Claim 4, wherein the gate electrode is extended onto the first insulation film.

7. The semiconductor device according to Claim 1, wherein the impurity concentration of the sub-region on the side of the second region is higher than the impurity concentration of the sub-region on the side of the third region.

8. The semiconductor device according to Claim 4, wherein the impurity concentration of the sub-region on the side of the second region is higher than the impurity concentration of the sub-region on the side of the third region.

9. The semiconductor device according to Claim 2, wherein the diffusion depth of the sub-region on the side of the second region is deeper than the diffusion depth of the sub-region on the side of the third region.

10. The semiconductor device according to Claim 5, wherein the diffusion depth of the sub-region on the side of the second region is deeper than the diffusion depth of the sub-region on the side of the third region.

11. The semiconductor device according to Claim 1, wherein the impurity concentration of the sub-region is the concentration of an impurity of the second conductivity type.

12. The semiconductor device according to Claim 4, wherein the impurity concentration of the sub-region is the concentration of an impurity of the second conductivity type.

13. The semiconductor device according to Claim 1, wherein the surface impurity concentration of the fifth region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the fifth region.

14. The semiconductor device according to Claim 4, wherein the surface impurity concentration of the fifth region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the fifth region.

15. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other;

selectively forming a fourth region of the first conductivity type in the surface portion of the second region;

selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region;

forming a first insulation film on the fifth region;

forming a gate electrode above the extended portion of the second region extending between the fourth region and the first region, with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

forming a first main electrode on the fourth region; and

forming a second main electrode on the third region;

wherein the step of selectively forming the fifth region comprises:

(1) introducing a predetermined amount of an impurity of the second conductivity type in the portion of the first region in which it is intended to form the fifth region;

(2) dividing the intended portion of the first region into a plurality of sub-regions;

(3) adding a further amount of the impurity of the second conductivity type to the sub-region nearer to the second region; and

(4) thermally driving the impurity in the sub-regions collectively.

16. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other;

selectively forming a fourth region of the first conductivity type in the surface portion of the second region;

selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region;

forming a first insulation film on the fifth region;

forming a gate electrode above the extended portion of the second region extending between the fourth region and the first region, with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

forming a first main electrode on the fourth region; and

forming a second main electrode on the third region;

wherein the step of selectively forming the fifth region comprises:

(1) introducing a predetermined amount of an impurity of the second conductivity type in the portion of the first region in which it is intended to form the fifth region;

(2) dividing the intended portion of the first region into a plurality of sub-regions;

(3) adding a further amount of the impurity of the second conductivity type to the sub-region nearer to the second region;

(4) introducing a further amount of an impurity of the first conductivity type to the sub-region nearer to the third region, the amount of the impurity of the first conductivity type being less than the predetermined amount of the impurity of the second conductivity type; and

(5) thermally driving the impurities in the sub-regions collectively.

17. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

selectively forming a second region of a second conductivity type and a third region of a first conductivity type in the surface portion of a first region of the first conductivity type, the second region and the third region being spaced apart from each other;

selectively forming a fourth region of the first conductivity type in the surface portion of the second region;

selectively forming a fifth region of the second conductivity type in the surface portion of the first region between the second region and the third region;

forming a first insulation film on the fifth region;

forming a gate electrode above the extended portion of the second region extending between the fourth region and the first region, with a gate insulation film interposed

between the extended portion of the second region and the gate electrode;

forming a first main electrode on the fourth region; and

forming a second main electrode on the third region;

wherein the step of selectively forming the fifth region comprises:

(1) dividing into a plurality of sub-regions that portion of the first region in which the fifth region is intended to be formed;

(2) introducing a further amount of an impurity of the first conductivity type to the sub-region nearer to the third region;

(3) introducing a predetermined amount of an impurity of the second conductivity type to the sub-regions, the predetermined amount of the impurity of the second conductivity type being more than the amount of the impurity of the first conductivity type; and

(4) thermally driving the impurities in the sub-regions collectively.

18. The method according to Claim 15, the method further comprising the step of extending the gate electrode onto the first insulation film.

19. The method according to Claim 16, the method further comprising the step of extending the gate electrode onto the first insulation film.

20. The method according to Claim 17, the method further comprising the step of extending the gate electrode onto the first insulation film.

21. The method according to Claim 15, the method further comprising the step of selectively forming the first region in the surface portion of a semiconductor substrate of the second conductivity type.

22. The method according to Claim 16, the method further comprising the step of selectively forming the first region in the surface portion of a semiconductor substrate of the second conductivity type.

23. The method according to Claim 17, the method further comprising the step of selectively forming the first region in the surface portion of a semiconductor substrate of the second conductivity type.

24. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

forming a mask for ion implantation, the mask having an opening and the area of the opening becoming wider toward a semiconductor substrate;

implanting impurity ions into the surface portion of the semiconductor substrate below the opening of the mask; and

thermally driving the implanted impurity ions, thereby forming an impurity diffusion region in the semiconductor substrate.

25. The method according to Claim 24, wherein the step of forming comprises

(1) laminating a plurality of layers on the semiconductor substrate and (2) etching the layers, one by one, from the uppermost layer to the lowermost layer and using each upper layer as a mask for etching the successively lower layer, thereby forming a wider opening in each lower layer.

26. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

forming an oxide film on a semiconductor substrate;

coating a photoresist on the oxide film;

positioning a photomask on the photoresist;

selectively forming an opening in the photoresist through the photomask;

removing that portion of the oxide film beneath the opening of the photoresist and that portion of the oxide film within a predetermined lateral range from the edge of the opening of the photoresist, using the photoresist as a mask;

implanting impurity ions through the opening of the photoresist, the oxide film and the photoresist, whereby to implant the impurity ions into the surface portion of the semiconductor substrate beneath the opening of the photoresist, the surface portion of the semiconductor substrate beneath the photoresist but not covered by the oxide film, and the surface portion of the semiconductor substrate beneath the oxide film; and

thermally driving the implanted impurity ions, thereby forming an impurity diffusion region in the semiconductor substrate.

27. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

forming an oxide film on a semiconductor substrate;

forming a nitride film on the oxide film;

coating a photoresist on the nitride film;

curing the photoresist;

selectively forming an opening in the photoresist by photolithography;

removing the portion of the nitride film beneath the opening of the photoresist, thereby forming an opening in the nitride film;

removing the portion of the oxide film beneath the opening of the nitride film and the portion of the oxide film within a predetermined lateral range from the edge of the opening of the nitride film using the nitride film as a mask, thereby forming an opening in the oxide film;

implanting boron ions into the entire surface portion of the semiconductor substrate using the photoresist, the nitride film and the oxide film as a mask;

removing the mask formed by the photoresist, the nitride film and the oxide film; and

thermally driving the implanted boron ions, thereby forming an impurity diffusion region in the semiconductor substrate.

28. A method of manufacturing a semiconductor device exhibiting a high breakdown voltage, the method comprising the steps of:

forming an oxide film on a semiconductor substrate;

forming a nitride film on the oxide film;

coating a photoresist on the nitride film;

positioning a photomask on the photoresist;

selectively forming an opening in the photoresist through the photomask;

removing the portion of the nitride film beneath the opening of the photoresist and that portion of the nitride film within a predetermined lateral range from the edge of the opening of the photoresist, using the photoresist as a mask;

implanting impurity ions of a first conductivity type into the semiconductor substrate using the photoresist as a mask;

removing the photoresist;

thermally treating the portion of the oxide film not covered by the nitride film, thereby forming a selectively oxidized film;

removing the nitride film;

implanting impurity ions of a second conductivity type into the semiconductor substrate using the selectively oxidized film as a mask; and

thermally driving the implanted impurity ions of the first conductivity type and the implanted impurity ions of the second conductivity type, thereby forming an impurity diffusion region of the first conductivity type and an impurity diffusion region of the second conductivity type in the semiconductor substrate.